ENGLISH

TRANSLATION

OF INTERNATIONAL

APPLICATION AS FILED

DESCRIPTION

CURRENT DIRECTION DETECTION CIRCUIT AND SWITCHING

REGULATOR HAVING THE SAME

TECHNICAL FIELD

[0001]   The present invention relates to a current

direction detection circuit that, when reverse direction

current flows in an earth side output transistor, is capable

of detecting the flow of current, and to a switching

regulator comprising this current direction detection

circuit.

BACKGROUND ART

[0002]   A switching regulator is provided with a power

source side output transistor that constitutes a main

switching element, between a terminal that inputs power and a

terminal that is connected with the load and outputs a

predetermined DC voltage, and maintains a predetermined DC

voltage by turning on/off (conductive/non-conductive) this

power source side output transistor. Such regulators are of

small size and are capable of achieving high power efficiency

and so are widely used. In recent years, synchronous

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rectifying switching regulators have come to be used (see for example Patent Document 1), in which an earth side output transistor is additionally provided, constituting a synchronous rectifying switching element. Such synchronous rectifying switching regulators make it possible to further improve power efficiency.

[0003]   Figure 3 shows the layout of a conventional synchronous rectifying switching regulator. This switching regulator 101 includes a power source side output transistor 111 constituted by a P type MOS transistor and an earth side output transistor 112 constituted by an N type MOS transistor connected in series between the input power source V_{cc} and earth potential, a smoothing circuit 113 whose input terminal is connected to a point between the two transistors 111, 112 and whose output terminal is connected with the output terminal OUT, respectively, a regulator control circuit 115 that outputs a control signal A and control signal B that perform on/off control of the power source side output transistor 111 and earth side output transistor 112 so as to maintain a predetermined DC voltage in response to feedback input of the voltage of the output terminal OUT, a current direction detection circuit 116 that, when reverse direction

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current flows in the earth side output transistor 112, detects this and outputs a control signal F, and an earth side output transistor control circuit 117 that outputs an output signal C for controlling the earth side output transistor 112 in accordance with the control signal B and control signal F. In this case, a load 114 is connected at the outside to the output terminal OUT. Also, the smoothing circuit 113 includes a smoothing coil 140 having one terminal connected with the connection point (node D) of the power source side output transistor 111 and the earth side output transistor 112 and the other terminal connected with the output terminal OUT, and a smoothing capacitor 141 having one terminal connected with the output terminal OUT and the other terminal earthed. Also, the control signal A and the control signal B that are output by the regulator control circuit 115 have practically the same waveform.

[0004]   The current direction detection circuit 116 includes a comparator 120 that performs comparison by respectively inputting the voltage of the node D at its inversion input terminal and earth potential at its non-inversion input terminal. Also, the earth side output transistor control circuit 117 includes an AND circuit 130

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that inputs the control signal B of the regulator control
circuit 115 and the control signal F of the current direction
detection circuit 116 and a buffer 131 that delivers output
with raised current capability.

[0005]   Next, the operation of the switching regulator 101
will be described with reference to Figure 4. In this
Figure, V_B is the voltage of the control signal B of the
regulator control circuit 115, V_C is the voltage of the
output signal C of the earth side output transistor control
circuit 117, I_O is the current flowing in the earth side
output transistor 112, and V_D is the voltage at the node D.
It should be noted that this Figure shows the waveform when
the load 114 is light, the case where the load 114 is large
is not shown.

[0006]   In the period in which control signal B is low
level, the output signal C is low level, and the earth side
output transistor 112 is turned off. The control signal A is
also low level, so the power source side output transistor
111 is turned on. Consequently, the current I_O flowing in
the earth side output transistor 112 is zero, and the voltage
V_D at the node D is high level.

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[0007]   Since, when the control signal B is high level, the control signal A is also high level, the power source side output transistor 111 is turned off. When the voltage V_D at the node D drops, becoming lower than the earth potential, the control signal F becomes high level, with the result that the earth side output transistor 112 is turned on. In this way, first of all current I_O in the positive direction flows from earth potential to the node D. When this happens, the voltage V_D at the node D drops from earth potential by an amount of the voltage that is acquired by multiplying this current I_O and the on- resistance of the earth side output transistor 12.

[0008]   After this, the current I_O gradually decreases linearly, and, in response thereto, the negative voltage V_D at the node D gradually rises in linear fashion. If the load 114 is large (not shown), the initial current value prior to commencement of decrease of the current I_O is large, so, before this current I_O will become a current in the reverse direction, the control signal B returns to low level after the lapse of a period in which the control signal B is high level. In contrast, if the load 114 is light, the current I_O becomes a current in the reverse direction before the high

level period of the control signal B has lapsed. This reverse direction current is a current that flows out towards the earth potential, so it represents a power loss and the power efficiency of the switching regulator 101 is lowered to that extent. Accordingly, when the current becomes a reverse direction current, this is detected by the current direction detection circuit 116, which outputs a low level control signal F. As a result, the voltage V_C of the output signal C becomes low level and the earth side output transistor 112 is thereby forcibly turned off, so that the flow of this current in the reverse direction is suppressed.

[0009]   Patent Document 1: Japanese Patent Application Laid-open No. 2000-92824

DISCLOSURE OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0010]   Thus, when the load is light, the earth side output transistor 112 is forcibly turned off when the current I_0 flows in the reverse direction, thereby making it possible to raise the power efficiency. The inventor of the present application, as a result of studies directed at achieving further improvements in power efficiency, noted that there is

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a certain delay (period t_0 in Figure 4) from detection of the reverse direction current of the earth side output transistor 112 by the current direction detection circuit 116, before this transistor is turned off, and this delay allows a reverse direction current to flow for a certain period, which therefore results in power loss. Also, since the voltage V_D at the node D has a wide range of variation from the power source voltage to below earth potential, the comparator 120 of the current direction detection circuit 116, which has as its input voltage a voltage of such a wide range of variation, must be larger in terms of the scale of its circuitry compared with an ordinary comparator, whose input voltage is a voltage of narrow range of variation.

[0011]   Also, with this switching regulator 101, as shown in Figure 4, there is a risk that swing i.e. ringing of the gradually decaying voltage generated after the forcible turning off of the earth side output transistor 112 will cause the voltage V_D at the node D to drop below earth potential, resulting in instantaneous activation of the current direction detection circuit 116, with consequent wasted power consumption or generation of noise.

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[0012]   The present invention was made in view of the above circumstances. Its object is to provide a current direction detection circuit wherein even better suppression of power losses can be achieved by being used for a switching regulator and so on and in which small circuit scale can be provided. Another object is to provide a switching regulator in which current losses can be suppressed by such a current direction detection circuit and wherein there is no possibility of reactivation of the current direction detection circuit after detection of a reverse direction current.

MEANS FOR SOLVING THE PROBLEM

[0013]   In order to solve the above problem, a current direction detection circuit according to a preferred embodiment of the present invention for detecting flow of current in the reverse direction in an earth side output transistor, through which current flows from an earthed input terminal to the output terminal, comprises a monitoring transistor having a control terminal and an output terminal respectively connected with a control terminal and an output terminal of the earth side output transistor, an impedance

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element having one terminal connected with the input terminal of the monitoring transistor and the other terminal earthed, first and second constant-current sources, a diode-connected reference transistor interposed between the first constant-current source and earth potential, and a sensing transistor, interposed between the second constant-current source and the impedance element, having a control terminal connected with a control terminal of the reference transistor, wherein the voltage between the second constant-current source and sensing transistor is output as a control signal to control the earth side output transistor and monitoring transistor.

[0014]   A switching regulator according to a preferred embodiment of the present invention comprises a power source side output transistor and a earth side output transistor provided in series between an input power source and earth potential, a smoothing circuit having an input terminal connected between the power source side output transistor and the earth side output transistor and an output terminal connected with a switching regulator output terminal that outputs a predetermined DC voltage, a regulator control circuit that performs on/off control of the power source side output transistor and earth side output transistor so as to

maintain a predetermined DC voltage by inputting as feedback the voltage of the switching regulator output terminal, the current direction detection circuit according to claim 1, and an earth side output transistor control circuit that controls the earth side output transistor so as to maintain the same continually turned off once the control signal of the current direction detection circuit has risen, after being turned on by the control signal of the regulator control circuit.

EFFECTS OF THE INVENTION

[0015]   In the current direction detection circuit according to the preferred embodiment of the present invention, as described above, by the configuration of the monitoring transistor, the impedance element, the first and second constant-current sources, the reference transistor and the sensing transistor, the control signal is output on detection of the condition a little prior to the point where the current flowing in the earth side output transistor starts to flow in the reverse direction, so it becomes possible to further suppress the power loss thereof by being used for a switching regulator and so on, and furthermore the scale of the circuitry can be made smaller. Also, in the

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switching regulator according to the preferred embodiment of
the present invention, the current direction detection
circuit cannot be reactivated after detection of the current
in the reverse direction, so wasted power consumption
produced by ringing or generation of noise can be suppressed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] [Fig. 1] Fig.1 is a circuit diagram of a current
direction detection circuit according to an embodiment of the
present invention and a switching regulator comprising this.

[Fig. 2] Fig.2 is an operating waveform diagram of the
above.

[Fig. 3] Fig.3 is a circuit diagram of a switching
regulator according to the background art.

[Fig. 4] Fig.4 is an operating waveform diagram of the
above.

EXPLANATION OF REFERENCE NUMERALS

[0017] 1 switching regulator

11 power source side output transistor

12 earth side output transistor

13 smoothing circuit

11

14 load

15 regulator control circuit

16 current direction detection circuit

17 earth side output transistor control circuit

20 monitoring transistor

21 impedance element

22 first constant-current source

23 second constant-current source

24 reference transistor

25 sensing transistor

V_{cc} input power source

OUT output terminal

BEST MODE FOR CARRYING OUT THE INVENTION

[0018]   A best mode of the present invention is described below with reference to the drawings. Figure 1 is a circuit diagram of a current direction detection circuit and a switching regulator comprising this according to an embodiment of the present invention. This switching regulator 1 includes a power source side output transistor 11 constituted by a P type MOS transistor and an earth side output transistor 12 constituted by an N type MOS transistor

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connected in series between the input power source V_{cc} and

earth potential, a smoothing circuit 13 having an input

terminal connected between the two transistors 11, 12 and an

output terminal connected to the output terminal (switching

regulator output terminal) OUT, a regulator control circuit

15 that outputs a control signal A and control signal B that

perform on/off control of the power source side output

transistor 11 and earth side output transistor 12 so as to

maintain a predetermined DC voltage by inputting as feedback

the voltage of the output terminal OUT, a current direction

detection circuit 16 that, when reverse direction current

flows in the earth side output transistor 12, detects this

and outputs a control signal F, and an earth side output

transistor control circuit 17 that outputs an output signal C

for controlling the earth side output transistor 12 by means

of the control signal B and control signal F. A load 14 is

connected at the outside to the output terminal OUT. Also,

the smoothing circuit 13 includes a smoothing coil 40 having

one terminal connected with the connection point (node D) of

the power source side output transistor 11 and the earth side

output transistor 12 and the other terminal connected with

the output terminal OUT, and a smoothing capacitor 41 having

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one terminal connected with the output terminal OUT and the other terminal earthed. Also, the control signal A and the control signal B that are output by the regulator control circuit 15 have practically the same waveform.

[0019]   The current direction detection circuit 16 includes a monitoring transistor 20 constituted by an N type MOS transistor having the gate (control terminal) and drain (output terminal) respectively connected with the gate (control terminal) and drain (output terminal) of the earth side output transistor 12, an impedance element 21 having one terminal connected with the source (input terminal) of the monitoring transistor 20 and the other terminal earthed, first and second constant-current sources 22, 23 each constituted by a P-type MOS transistor, a reference transistor 24, interposed between the first constant-current source 22 and earth potential, that is constituted by a diode-connected (i.e. having its drain and gate mutually connected) N type MOS transistor, and a sensing transistor 25 constituted by an N type MOS transistor, interposed between the second constant-current source 23 and impedance element 21, having a gate (control terminal) connected to the gate (control terminal) of the reference transistor. Also, the

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current direction detection circuit 16 includes a P-type MOS transistor 26 constituting a current mirror circuit with the first and second constant-current sources 22, 23 and setting the current values of these, and a constant-current source 27 that generates the current that flows to the P-type MOS transistor 26. The current direction detection circuit 16 outputs as a control signal the voltage between the second constant-current source 23 and sensing transistor 25 (i.e. at the node F) and thereby controls the earth side output transistor 12 and the monitoring transistor 20 via the earth side output transistor control circuit 17.

[0020]   Since the monitoring transistor 20 passes a current that is comparatively small in proportion to the current value of the earth side output transistor 12, it is set to a size of 1/N of the earth side output transistor 12 (N is a predetermined value). The impedance element 21 is an element that generates a voltage in response to the current that flows therein and for this impedance element 21 there may be used for example a resistor or an N type MOS transistor whose on-resistance is set to a comparatively high value. The first constant-current source 22 and second constant-current source 23 have the capability of passing equal constant

currents I_{REF} (for example 1 μA). Also, the size of the reference transistor 24 is set such that the connection point of the first constant-current source 22 and reference transistor 24 is high level. Then, in case the sizes of the reference transistor 24 and sensing transistor 25 are equal, if the voltage V_E at the node E is substantially at least earth potential, the voltage V_F at the node F (i.e. the voltage of the control signal that is output by the current direction detection circuit 16) is high level. In contrast, when the voltage V_E at the node E drops substantially below the earth potential, the on-resistance of the sensing transistor 25 falls, with the result that the voltage V_F at the node F becomes low level.

[0021]   More specifically, the case where the voltage at the node E is at least earth potential includes the case where the monitoring transistor 20 is off and the case where the monitoring transistor 20 is on, but the voltage V_D at the node D is at least earth potential. If the monitoring transistor 20 is off, current tries to flow from the second constant-current source 23 to the impedance element 21 (for example 1 KΩ), so the voltage at the node E rises slightly from earth potential. Also, if the monitoring transistor 20

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is on and the voltage V_D at the node D is at least earth potential, current flows through the monitoring transistor 20 and impedance element 21 from the node D, so the voltage V_E at the node E becomes a value obtained by dividing the voltage V_D at the node D by the on resistance of the monitoring transistor 20 and the resistance of the impedance element 21. In contrast, more specifically, the case where the voltage V_E at the node E drops below earth potential represents the case where the monitoring transistor 20 is on and the voltage V_D at the node D is a voltage that is lower than earth potential i.e. negative voltage. In this case, since the current flows from earth potential through the impedance element 21 and monitoring transistor 20, the voltage V_E at the node E is a value obtained by dividing the negative voltage V_D at the node D by the resistance of the impedance element 21 and the on resistance of the monitoring transistor 20.

[0022]   Even more strictly, even in the case where the monitoring transistor 20 is on and the node D has a negative voltage, if this negative voltage value is small, the voltage V_E at the node E may be earth potential or more. That is, if for example the "on" resistance value of the monitoring

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transistor 20 and the resistance value of the impedance

element 21 are both set at R, the voltage V_E at the node E is

$$V_E = (V_D + I_{REF} \times R)/2.$$

As stated above, I_{REF} is the constant current value of the

second constant-current source 23. Since, when $V_D = - I_{REF} \times$

R, V_E is zero, even if the voltage V_D at the node D is

negative if it is smaller than $(I_{REF} \times R)$, the voltage V_E at

the node E is at least earth potential. Thus, the voltage V_D

at the node D has an offset in the negative direction from

the earth potential and is detected by the current direction

detection circuit 16. The value of this offset can be

adjusted by means of I_{REF} or the resistance value of the

impedance element 21. Using this, the fact that current in

the reverse direction is about to flow in the earth side

output transistor 12 can be detected a little before this

actually happens. But, this will be described later.

[0023]   Next, the earth side output transistor control

circuit 17 will be described. The earth side output

transistor control circuit 17 includes an OR circuit 30 that

inputs the inverted signal of the control signal B of the

regulator control circuit 15 and a control signal F of the

current direction detection circuit 16, an edge detection

circuit 31 that inputs the control signal B at its set input terminal S, inputs the output of the OR circuit 30 at its reset input terminal R and outputs the result from the non-inversion output terminal Q, and a buffer 32 that delivers the output of the edge detection circuit 31 with increased current capability. The edge detection circuit 31 outputs high level from its non-inversion output terminal Q in response to the rising edge of the input signal of the set input terminal S, and maintains this condition, and outputs low level from its non-inversion output terminal Q in response to the rising edge of the input signal of the reset input terminal R, and maintains this condition.

[0024]   Next, the operation of the switching regulator 1 will be described with reference to Figure 2, focusing on the operation of the current direction detection circuit 16. In this Figure, V_B is the voltage of the control signal B of the regulator control circuit 15, V_C is the voltage of the output signal C of the earth side output transistor control circuit 17, I_O is the current flowing in the earth side output transistor 12, V_D is the voltage at the node D, V_E is the voltage at the node E, and V_F is the voltage of the control signal F of the current direction detection circuit 16. The

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height of V_E in this Figure is shown to a larger scale.

Also, this Figure shows the waveform when the load 14 is

light. The case where the load 14 is large is not shown.

[0025]　　In the period in which the control signal B is low

level, the output signal C is low level and the earth side

output transistor 12 and monitoring transistor 20 are turned

off.　The control signal A is also low level and the power

source side output transistor 11 is turned on.　Consequently,

the current I_O flowing in the earth side output transistor 12

is zero, and the voltage V_D at the node D is high level.　The

monitoring transistor 20 is off, so, as described above, the

voltage V_E at the node E is raised slightly from the earth

potential, causing the voltage V_F at the node F to become

high level.

[0026]　　When the control signal B becomes high level, the

control signal A also becomes high level, so the power source

side output transistor 11 is turned off.　The earth side

output transistor control circuit 17 then outputs high level

on receiving the rising edge of the control signal B, thereby

turning the earth side output transistor 12 and monitoring

transistor 20 on.　In response to turning on of the earth

side output transistor 12, first of all, a current I_O in the

positive direction flows from earth potential to the node D. When this happens, the voltage V_D at the node D is lowered from earth potential by an amount of the voltage that is acquired by multiplying this current I_0 and the on-resistance of the earth side output transistor 12. The voltage V_E at the node E is also a negative voltage, and the voltage V_F at the node F becomes low level.

[0027] After this, the current I_0 gradually decreases linearly, and in response to this the negative voltage V_D at the node D and the voltage V_E at the node E gradually increase linearly. Thereupon, if the load 14 is large (not shown), the initial current value is large prior to the commencement of decrease of the current I_0, so, before this current I_0 will become a current in the reverse direction, the control signal B returns to low level after the lapse of the high level period. In this case, the earth side output transistor control circuit 17 delivers low level output on receipt of the trailing edge of the input control signal B, with the result that the earth side output transistor 12 and monitoring transistor 20 are turned off (not shown).

[0028] In contrast, when the load 14 is light, the current I_0 flowing in the earth side output transistor 12 tries to

become a reverse direction current and the voltage V_D at the node D tries to become positive voltage before the lapse of the high level period of the control signal B. However, as described above, since the voltage V_D at the node D has an offset in the negative direction from earth potential, this situation is detected by the current direction detection circuit 16. In other words, the current direction detection circuit 16 detects the condition slightly prior to the current I_O becoming a current in the reverse direction, and outputs a high level control signal at the node F. On receipt of the rising edge of this input control signal F of the current direction detection circuit 16, the earth side output transistor control circuit 17 then outputs low level and thereby forcibly turns the earth side output transistor 12 off. Specifically, the earth side output transistor control circuit 17 effects control of the earth side output transistor 12 such that this output transistor 12 continues to be turned off once the control signal F of the current direction detection circuit 16 has risen after being turned on by the control signal B of the regulator control circuit 15.

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[0029]   Thus, by detection of this situation a little prior to the flow of current in the reverse direction in the earth side output transistor 12, the current direction detection circuit 16 compensates for the circuit delay produced by the current direction detection circuit 16 and the earth side output transistor control circuit 17 and so suppresses power loss, thereby making it possible to increase the power efficiency. Compared with the current direction detection circuit 116 of the background art, whose input voltage is a voltage of wide range of variation used in the switching regulator 101, the current direction detection circuit 16 is of concise circuit construction and uses an input voltage of narrow range of variation. The scale of this current direction detection circuit 16 can therefore be made small.

[0030]   When the earth side output transistor 12 is forcibly turned off, the voltage V_D at the node D converges with ringing to the voltage level of the output terminal OUT and then is stabilized. However, when this happens, the earth side output transistor control circuit 17 controls the earth side output transistor 12 such that this earth side output transistor 12 remains turned off once the control signal F of the current direction detection circuit 16 has risen, so

there is no risk of reactivation of the current direction detection circuit 16 by ringing, such as could occur in the switching regulator 101 in the background art.

[0031] It should be noted that, although the current direction detection circuit according to this embodiment of the present invention was devised for a switching regulator, it could also be used in other devices having an earth side output transistor that outputs current to a coil (such as for example a motor drive device).

[0032] Also, the present invention is not restricted to the embodiment described above and various design modifications are possible within the scope of the claims.